AMENDMENT

Please amend the application as follows:

In the Claims:

Please cancel claims 34-78 (claim 2 was canceled previously). The claims and their status follow:

1. (Original) A receiver digital circuitry, comprising:

digital down-converter circuitry configured to mix a digital input signal provided by a receiver analog circuitry with an intermediate frequency (IF) local oscillator signal to generate a digital down-converted signal; and

digital filter circuitry configured to filter the digital down-converted signal to generate a filtered digital signal,

wherein the receiver analog circuitry resides within a first integrated circuit, and

wherein the receiver digital circuitry resides within a second integrated circuit, and the second integrated circuit couples to the first integrated circuit via a one-bit digital interface.

2. (Cancelled.)

3. (Previously presented) The receiver digital circuitry of claim 1, wherein the digital filter circuitry comprises a channelization filter circuitry.

4. (Previously presented) The receiver digital circuitry of claim 3, wherein the digital input signal comprises a digital in-phase signal and a digital quadrature signal.

5. (Previously presented) The receiver digital circuitry of claim 4, wherein the channelization filter circuitry comprises a cascade coupling of a cascade integrator/comb (CIC) filter circuitry and a secondary filter circuitry.

6. (Previously presented) The receiver digital circuitry of claim 5, wherein the cascade integrator/comb filter circuitry comprises a cascade coupling of an integrator chain circuitry, a decimator circuitry, and a differentiator chain circuitry.

7. (Previously presented) The receiver digital circuitry of claim 6, wherein the channelization filter circuitry provides a notch at minus a frequency of the intermediate frequency local oscillator signal.

8. (Previously presented) The receiver digital circuitry of claim 7, wherein the secondary filter circuitry includes a cascade coupling of a notch circuitry and at least one biquad filter circuitry.

9. (Previously presented) The receiver digital circuitry of claim 8, wherein the notch filter circuitry provides the notch at minus the frequency of the intermediate frequency local oscillator signal.

10. (Previously presented) The receiver digital circuitry of claim 9, wherein the intermediate frequency local oscillator signal comprises a digital signal.

11. (Previously presented) The receiver digital circuitry of claim 10, used within a radio-frequency transceiver circuitry.

12. (Previously presented) The receiver digital circuitry of claim 10, further comprising a digital programmable gain amplifier circuitry configured to provide a programmable gain applied to the filtered digital signal to produce a digital scaled signal.

13. (Previously presented) The receiver digital circuitry of claim 12, further comprising a digital-to-analog converter circuitry coupled to the digital programmable gain amplifier circuitry, the digital-to-analog converter circuitry configured to convert the digital scaled signal to an analog output signal.

14. (Previously presented) The receiver digital circuitry of claim 13, wherein the digital-to-analog circuitry is further configured to provide the analog output signal to a baseband processor circuitry coupled to the receiver digital circuitry.

15. (Previously presented) The receiver digital circuitry of claim 14 used within a radio-frequency transceiver circuitry.

16. (Previously presented) A receiver digital circuitry, comprising:

digital filter circuitry configured to filter a digital input signal provided by a receiver analog circuitry to generate a filtered digital signal; and

digital down-converter circuitry configured to mix the filtered digital signal with an intermediate frequency (IF) local oscillator signal to generate a digital down-converted signal; and

wherein the receiver analog circuitry resides within a first integrated circuit, and

wherein the receiver digital circuitry resides within a second integrated circuit, and the second integrated circuit couples to the first integrated circuit via a one-bit digital interface.

17. (Previously presented) The receiver digital circuitry of claim 16, wherein the digital filter circuitry comprises a channelization filter circuitry.

18. (Previously presented) The receiver digital circuitry of claim 17, wherein the digital input signal comprises a digital in-phase signal and a digital quadrature signal.

19. (Previously presented) The receiver digital circuitry of claim 18, wherein the channelization filter circuitry comprises a cascade coupling of a cascade integrator/comb (CIC) filter circuitry and a secondary filter circuitry.

20. (Previously presented) The receiver digital circuitry of claim 19, wherein the cascade integrator/comb filter circuitry comprises a cascade coupling of an integrator chain circuitry, a decimator circuitry, and a differentiator chain circuitry.

21. (Previously presented) The receiver digital circuitry of claim 20, wherein the channelization filter circuitry provides a notch at zero frequency.

22. (Previously presented) The receiver digital circuitry of claim 21, wherein the secondary filter circuitry includes a cascade coupling of a notch circuitry and at least one biquad filter circuitry.

23. (Previously presented) The receiver digital circuitry of claim 22, wherein the notch filter circuitry provides the notch at zero frequency.

24. (Previously presented) The receiver digital circuitry of claim 23, wherein the intermediate frequency local oscillator signal comprises a digital signal.

25. (Previously presented) The receiver digital circuitry of claim 24, used within a radio-frequency transceiver circuitry.

26. (Previously presented) The receiver digital circuitry of claim 24, further comprising a digital programmable gain amplifier circuitry configured to provide a programmable gain applied to the digital down-converted signal to produce a digital scaled signal.

27. (Previously presented) The receiver digital circuitry of claim 26, further comprising a digital-to-analog converter circuitry coupled to the digital programmable gain amplifier circuitry, the digital-to-analog converter circuitry configured to convert the digital scaled signal to an analog output signal.

28. (Previously presented) The receiver digital circuitry of claim 27, wherein the digital-to-analog circuitry is further configured to provide the analog output signal to a baseband processor circuitry coupled to the receiver digital circuitry.

29. (Previously presented) The receiver digital circuitry of claim 28, used within a radio-frequency transceiver circuitry.

30. (Previously presented) The receiver digital circuitry of claim 24, further comprising a digital programmable gain amplifier coupled between the digital filter circuitry and the digital down-converter circuitry, the digital programmable gain amplifier circuitry configured to apply programmable gain to the digital filtered signal to produce a digital scaled signal, the digital programmable gain amplifier circuitry further configured to provide the digital scaled signal to the digital down-converter circuitry.

31. (Previously presented) The receiver digital circuitry of claim 30, further comprising a digital-to-analog converter circuitry coupled to the digital down-converter circuitry, the digital-to-analog converter circuitry configured to convert the digital down-converted signal to an analog output signal.

32. (Previously presented) The receiver digital circuitry of claim 31, wherein the digital-to-analog circuitry is further configured to provide the analog output signal to a baseband processor circuitry coupled to the receiver digital circuitry.

33. (Previously presented) The receiver digital circuitry of claim 32, used within a radio-frequency transceiver circuitry.

34-78. (Cancelled.)